Woody International Publish Limited
An Multidisciplinary Academic Journal Publisher

Journal of Artificial Intelligence and Information, Volume 1, 2024
https://www.woodyinternational.com/

CMOS Wide-Bandwidth Transimpedance Amplifier (TIA) at 5Gbps

Yihan Wang, You Zhang, Tianyuan Xu, Chenhao Ma, Justin Zhang

University of Michigan, Ann Arbor
{wangyhhh, youzh, tyxu, chenhaom, zjustin}@umich.edu

Abstract: ***A transimpedance amplifier (TIA) is an essential component in optical communication systems, serving as a current-to-voltage converter that amplifies the small current output from sensors such as photodetectors into a usable voltage signal. In high-speed optical communication, particularly at data rates such as 5 Gbps, the TIA's design becomes critical due to stringent bandwidth and noise performance requirements. This paper presents the design and implementation of a CMOS-based wide bandwidth TIA tailored for optical fiber communication operating at 5 Gbps. The design focused on achieving a bandwidth of at least 3.5 GHz, which is 0.7 times the data rate, to minimize pattern-dependent jitter and enhance the signal-to-noise ratio (SNR). This bandwidth is crucial to ensure signal integrity and reliable data transmission in high-speed optical links. The proposed TIA leverages CMOS technology for its advantages in low power consumption, high integration capability, and cost-effectiveness. Key design considerations include optimizing the feedback resistor and the input capacitance to achieve the desired bandwidth while maintaining low input-referred noise. Additionally, techniques to enhance linearity and stability across the wide frequency range are discussed. Simulation results demonstrate that the designed TIA meets the required performance criteria, offering a promising solution for integration in next-generation optical communication systems. Future work will focus on further reducing noise and power consumption while exploring the potential of scaling the design for even higher data rates. To prove why we only need 3.5GHz bandwidth to in a 5 Gbps system, we have Shannor's Capacity Theorem which states that: C= B log2(1 + S/N). Where C is Data Rate, B is Bandwidth, S/N is signal-to-noise power ratio. When S/N is 1.692 and bandwidth is 3.5 GHz, the Data Rate can meet the 5 Gps requirement and the bandwidth will also be at least 0.7 of the Data Rate.***

Cited as: Wang, Y., Zhang, Y., Xu, T., Ma, C., & Zhang, J. (2024). CMOS Wide-Bandwidth Transimpedance Amplifier (TIA) at 5Gbps. *Journal of Artificial Intelligence and Information*, *1*, 58–70. Retrieved from https://woodyinternational.com/index.php/jaii/article/view/55.

1. Introduction

In the design of high-speed optical communication systems, the performance of the transimpedance amplifier (TIA) is critical, especially when dealing with the large capacitance associated with current sources like photodiodes (I_{pd}). The challenge lies in maintaining a wide bandwidth while ensuring minimal signal distortion and noise, which are essential for reliable data transmission at high data rates, such as 5 Gbps. Given the relationship between bandwidth and the RC time constant ($\omega = \frac{1}{\rho RC}$), it's crucial to carefully manage the input impedance and the associated capacitance.

To address the issue of large photodiode capacitance, we opted for a common gate amplifier configuration. The common gate amplifier is known for its low input impedance that approximate ($\frac{1}{g_m}$), making it an ideal inductor for lowering the effects of the large capacitance of Ipd on the overall bandwidth. Yet, the drawback of this method is that regarding maintaining low impedance, either high direct current or large transistor width will limit the performance.

In this condition, we chose to implement the Regulated Cascode (RGC) architecture to overcome CG drawback. The RGC architecture modified the topology of CG as an isolation, giving the possibility of reducing power consumption and decreasing size of transistor while boosting transconductance. This isolation is achieved through the use of a feedback loop that stabilizes the operating point of the cascode transistor, thereby reducing the capacitive loading and improving the bandwidth.

For the differential stage of the TIA, we planned to use a differential input-differential output topology. This

approach not only improves the common-mode noise rejection but also provides the flexibility to achieve the required gain by adjusting the transistor parameters. By carefully tuning the size and biasing of the transistors, we can optimize the gain while maintaining stability and linearity across the operating frequency range.

Regarding the output swing, which is a key factor in ensuring the TIA's compatibility with subsequent stages of the optical receiver, we considered incorporating a post-amplifier stage. This post-amplifier is designed to provide an output swing greater than 80 mV, which is sufficient for driving the next stage with minimal signal degradation. The architecture of the post-amplifier will be chosen to balance between gain, bandwidth, and power consumption, ensuring that the overall system performance meets the stringent requirements of high-speed optical communication.

In summary, our TIA design focuses on minimizing the adverse effects of photodiode capacitance on bandwidth, achieving adequate gain through a differential architecture, and ensuring sufficient output swing using a post-amplifier stage. These considerations are crucial for developing a high-performance TIA capable of supporting data rates up to 5 Gbps in optical communication systems.

2. Design Description

2.1 Photodiode

In this Design, we plan to use a photodiode as the source to complete the following simulation. It's crucial to understand the equivalent circuit to help us predict how the photodiode and related components will perform in real-world applications. The equivalent circuit of a photodiode is composed of four primary elements: a current source, a parallel PN juction, a parallel capacitor, a parallel resistor and a series resistor as depicted in figure 1. The ideal current source (I_{pd}) represents the photocurrent generated by the diode when exposed to the incident light, while the junction capacitance (C_J) associated with the depletion of the PN junction, significantly influences the photodiode's frequency response, particularly at higher frequencies. Ideally, the shunt resistance (R_1) should be infinite to ensure that the current source delivers its entire current to the load. This configuration allows the current-to-voltage ratio to be determined solely by the load resistance, minimizing the impact of parasitic effects on overall system performance. In real-world scenarios, deviations from this ideal can lead to power losses and reduced efficiency, but for most practical applications, these effects are negligible. The series resistance (R_2), which is generally low, typically does not pose significant challenges in photodiode system design. However, it can become more critical in high-precision or high-speed applications where even small resistive losses could affect performance. Therefore, understanding and controlling series resistance is important for optimizing the overall design, though it is often considered a secondary concern.

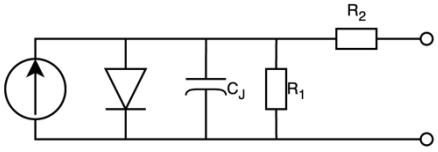

Figure 1: Equivalent Circuit of Photodiode

Given that the primary focus of this design is not on the photodiode itself but rather on other aspects of the system, we have chosen to simplify the photodiode model. By assuming infinite shunt resistance, zero series resistance, and ignoring the PN junction, we streamline the simulation process. This simplification allows us to dedicate more attention to other critical components and system behaviors, ensuring that the overall design meets its performance goals without unnecessary complexity in the photodiode modeling. Despite these simplifications, the model remains robust enough to provide accurate insights into the system's performance under various conditions.

2.2 Conventional Regulated Cascode (RGC)

The Regulated Cascode (RGC) configuration is widely used in the design of transimpedance amplifiers (TIAs), particularly for applications requiring low input impedance and high bandwidth, compared with the tight trade-off between gain bandwidth and noise in the CG structure. The RGC architecture achieves these objectives by incorporating local feedback mechanisms that regulates the operating point of the cascode transistor. This regulation not only lowers the input impedance further but also stabilizes the circuit against variations in process, voltage, and temperature (PVT). This makes it a preferred choice in many high-speed optical communication

systems where maintaining signal integrity is paramount.

The Figure 2 (a) depicts a single-ended TIA based on the conventional RCG structure, in which the Photodiode is represented by a current source (I_{in}) parallel with a photodiode capacitance (C_{PD}) as we mentioned above.

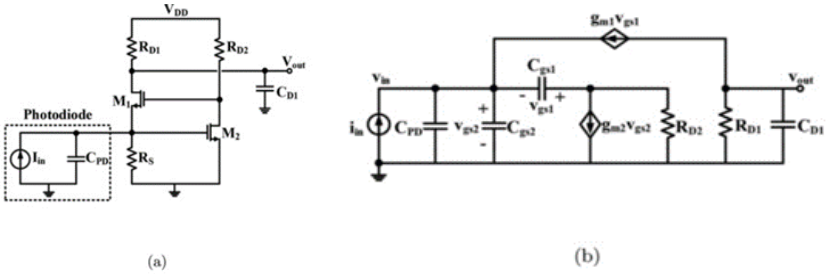

Figure 2: Conventional Regulated Cascode
(a) Schematic (b) Small Signal Module

Transistor M2 and Resistor R_{D2} together establish a local feedback loop, effectively reducing the input impedance by the value of its voltage gain of the loop. This reduction in input impedance mitigates the impact of the dominant pole formed at the input node, which arises from the substantial photodiode capacitance. In essence, the large capacitance of the photodiode is decoupled from the bandwidth-limiting factors. As a result, the transimpedance amplifier (TIA) experiences an improvement in bandwidth performance.

To facilitate the calculations required for sizing the design, Fig. 2(b) illustrates the small-signal model of the conventional resistive gate current (RGC) transimpedance amplifier. By applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL), we obtain the following equations:

$$v_{gs1} = -v \cdot \frac{1+g_{m2}R_{D2}}{1+sC_{gs1}R_{D2}} \tag{1}$$

$$v_{in} = \frac{i_{in}+v_{gs1}(g_{m1}+sC_{gs1})}{s(C_{gs2}+C_{pd})} \tag{2}$$

$$v_{out} = v_{gs1} \cdot \frac{g_{m1}R_{D1}}{1+sC_{D1}R_{D1}} \tag{3}$$

Where C_{gs1} is the gate-source capacitance of transistor M_1, while g_{m1} and g_{m2} refer to the transconductance of transistors M_1 and M_2, respectively. Given that $C_{PD} \gg C_{gs2}$ (i.e., the photodiode capacitance is significantly larger than the gate-source capacitance of transistor M_2), substituting Equation (1) into Equation (2) provides the following detailed expression for the input impedance of the conventional RGC TIA:

$$Z_{in}(s) = \frac{1+sC_{gs1}R_{D2}}{sC_{PD}(1+sC_{gs1}R_{D2})+(g_{m1}+sC_{gs1})(1+g_{m2}R_{D2})} \tag{4}$$

By inserting S = 0 in (4), the input impedance at low frequencies can be calculated as follows:

$$R_{in} = Z_{in}(0) = \frac{1}{g_{m1}(1+g_{m2}R_{D2})} \tag{5}$$

In (5), $g_{m2}R_{D2}$ is the voltage gain of the common-source stage formed by M_2 and R_{D2}. The conventional RGC TIA provides a small input resistance, which is a factor of $1/(1 + g_{m2}R_{D2})$ lower than that of CG TIA.

Also, by substituting (1) in (3), we have:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_{D1}(1+g_{m2}R_{D2})}{(1+sC_{gs1}R_{D2})(1+sC_{D1}R_{D1})} \tag{6}$$

So, the transimpedance gain of the conventional RGC TIA is obtained as follows:

$$ZT(s) = \frac{1}{(1+sC_{D1}R_{D1})} \frac{g_{m1}R_{D1}(1+g_{m2}R_{D2})}{[sC_{PD}(1+sC_{gs1}R_{D2})+(g_{m1}+sC_{gs1})(1+g_{m2}R_{D2})]} \tag{7}$$

which is equal to R_{D1} at low frequencies.

To further reduce the input impedance at the TIA input node, as described in Equation (5), the voltage gain of the

common-source (CS) stage, $g_{m2}R_{D2}$, should be increased. By enhancing the transconductance g_{m2} or the load resistance R_{D2}, the overall voltage gain can be amplified.

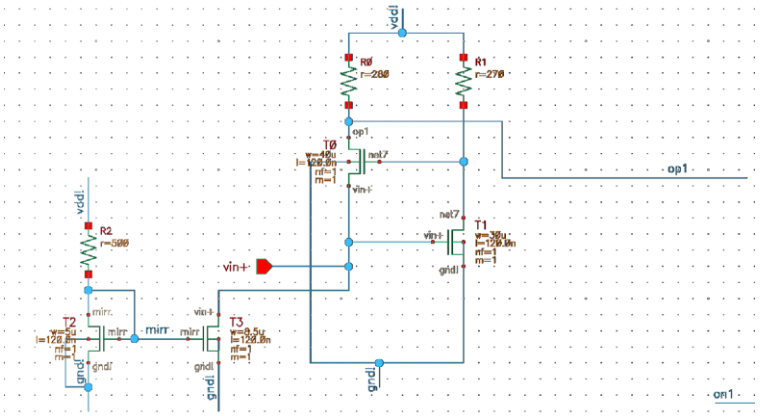

Figure 3: Conventional Regulated Cascode Schematic in Virtuoso with Parameters

Figure 3 shows the schematic of the conventional Regulated Cascode (RGC) transimpedance amplifier in Virtuoso, with labeled parameters.

To achieve a higher gain, R_{D1} (labeled as R_0 in the figure 3) is set to 280 Ω.

2.3 Common Drain

The Common-Drain amplifier, also known as a source follower, is recognized for its low output impedance. In contrast, the output impedance of a Common-Source stage is generally comparable to the MOS transistor's output resistance. Therefore, it is advantageous to include a buffer, such as a Common-Drain amplifier, between the output node and the Common-Source stage to effectively lower the overall output impedance and improve performance.

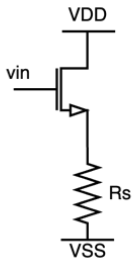

Figure 4: Common-Drain Amplifier

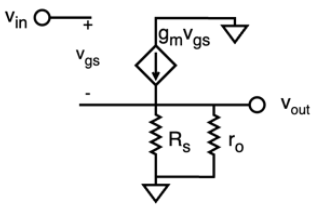

Figure 5: Common Drain Small Signal Model

Using the small signal model, we can derive the equations for the voltage gain and output impedance of the Common-Drain circuit shown in Figure 5, as given by Equations (8) and (9):

$$A_v = \frac{g_m r_s}{1+g_m r_s} \tag{8}$$

$$Z_{out} = R_S || \frac{1}{g_m} \tag{9}$$

In contrast to the Common-Source Amplifier, which offers significant voltage gain, the small signal gain of the

Common-Drain Amplifier is approximately unity and features a relatively low output impedance. As shown in Figure 4, the output voltage at the source closely follows the input voltage at the gate, which is why it is referred to as a "source follower."

2.4 Common Source (Gain Stage)

Common-Source amplifier could offer high input impedance, reducing loading on the previous stage, while also providing substantial voltage gain for signal amplification. To enhance the overall output gain in our design, we incorporated multiple stages of Common-Source amplifiers.

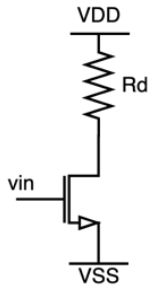

Figure 6: Common Source Amplifier

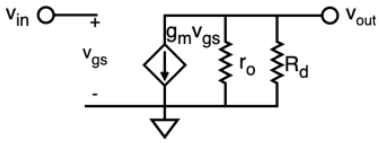

Figure 7: Common Source Small Signal Model

Using the small-signal model, we can derive the equations for the voltage gain and output impedance of the Common-Drain circuit shown in Figure 7. These are detailed in Equations (10) and (11).

$$A_v = -g_m(R_d||r_o) \tag{10}$$

$$Z_{out} = R_d||r_o \tag{11}$$

It is important to mention that small-signal definitions are only valid when the transistor operates in the saturation region, as it can then be approximated as a linear device for analysis.

To simplify, neglecting channel length modulation assumes the MOSFET has infinite output resistance (r_o), allowing us to use simplified equations for output resistance and voltage gain. Specifically, the output resistance equation becomes $Z_{out} = R_d$ and the voltage gain equation is $A_v = -g_m R_d$. To maximize the output gain, we should focus on increasing g_m and/or R_d.

2.5 How to Decide Gain Stages?

For the gain stage, we first need to determine the number of stages required to achieve the optimal bandwidth. After incorporating the RGC and common-drain buffer, we achieve a preliminary gain of approximately 250. To reach a total gain of 2.5K, we need to add gain stages such that the combined gain of these stages equals $\frac{2500}{250} = 10$ times the initial gain. Therefore, we should aim for stages which contributing a total gain of 10, to meet the overall gain requirement effectively.

We begin by assuming that replacing the single stage amplifier with a cascaded n-stage amplifier, while maintaining the same overall gain, allows us to express the relationship between the gain of the cascaded stages and the single-stage gain. Given the cascaded stage gain A_S and single stage gain A_0, we can establish the following equation:

$$A_S = \sqrt[n]{A_0} \tag{12}$$

Given the power dissipation of the cascaded stages, P_S, and the power dissipation of a single stage, P_0, we can express the total power dissipation for the cascaded system as:

$$P_S = \frac{P_0}{n} \tag{13}$$

Assuming that each Common-Source stage in the design has the same transfer function:

$$H(S) = \frac{A_S}{1+\frac{s}{\omega_S}} \tag{14}$$

Thus, the total transfer function would be the product of n stages, each described by Equation (14):

$$H_{total} = {H_S}^n = \frac{{A_S}^n}{\left(1+\frac{s}{\omega_S}\right)^n} \tag{15}$$

When $\omega=\omega_S$:

$$|H_S| = \frac{A_S}{\sqrt{2}} \tag{16}$$

By applying Equation (16) to Equation (15) and substituting s with ω_{3dB}, we can derive the 3dB bandwidth equation:

$$\begin{gathered} \left|H_{\omega_{3dB}}\right| = \frac{{A_S}^n}{\sqrt{2}} = \frac{{A_S}^n}{\left(1+\frac{\omega_{3dB}}{\omega_S}\right)^n} \\ \omega_{3dB} = \omega_S\left(2^{\frac{1}{n}}-1\right)^{\frac{1}{2}} \end{gathered} \tag{17}$$

As discussed above, in equation (10), the gain of the Common-Source amplifier is proportional to $g_m r_o$, g_m is also directly proportional to $\sqrt{I_D}$ (I_D is Drain Current), the output resistance r_o is proportional to $\frac{1}{I_D}$, indicating that the gain ultimately relates to $\frac{1}{\sqrt{I_D}}$. Furthermore, the main pole frequency ω_S, of the amplifier is defined as $\frac{1}{RC}$, where C is independent of I_D. Consequently, ω_S is also proportional to I_D. This relationship leads us to the following Equation (18):

$$GBW = A_S\omega_S \propto \frac{1}{\sqrt{I_D}} \times I_D = \sqrt{I_D} \tag{18}$$

Additionally, we know that $P_S = V_{DD}I_D$. Applying this relationship to Equation (18):

$$\begin{gathered} GBW \propto \sqrt{P_S} \\ P_S \propto GBW^2 \end{gathered} \tag{19}$$

Using Equations (19) and (13), we can derive the following results:

$${P_0}^2 = n^2 P_S \propto (A_0\omega_0)^2 = n^2(A_S\omega_S)^2 \tag{20}$$

The final gain bandwidth will be:

$$GBW = A_S\omega_S = \frac{1}{\sqrt{n}}A_0\omega_0 \tag{21}$$

By applying Equation (21) to Equation (17), we can derive the final equation for ω_{3dB}:

$$\omega_{3dB} = \frac{1}{n}A_0^{\left(1-\frac{1}{n}\right)}\omega_0\left(2^{\frac{1}{n}}-1\right)^{\frac{1}{2}} \tag{22}$$

Considering we need to achieve a gain of 10, using Equation (22), we find that for n is equal to 1, $\omega_{3dB} = \omega_0$. For n is equal to 2, $\omega_{3dB} = 1.02\ \omega_0$. For n is equal to 3, $\omega_{3dB} = 0.79\ \omega_0$. For n is equal to 4, $\omega_{3dB} = 0.61\ \omega_0$, and so on. It's important to note that the 3dB bandwidth will start decreasing after n is greater than 2. Therefore, we ultimately decide to implement two stages, each with a gain of approximately 3 to 4. This decision is based on the assumption that each stage has the same transfer function; however, we may not strictly follow this assumption when designing our gain stages.

2.6 Design Methodology

Our structure is essentially a differential Common-Source stage, so we initially decided to use a PMOS transistor as the active device to amplify the signal from the RGC, as shown in Figure 8. This choice was made because the DC output voltage of the RGC is approximately 1.2V, which is relatively high, making it difficult for an NMOS

transistor to operate in the saturation region.

In the design, we use an ideal current source to ensure the PMOS transistor remains in saturation while adjusting the W/L ratio to achieve the required gain. However, when we attempted to adjust the gain, we found it difficult to set the current as expected. This challenge arose primarily because the PMOS transistor, which functions as a current source, competes with the ideal current source we introduced, complicating the control of current and making it harder to achieve the desired performance.

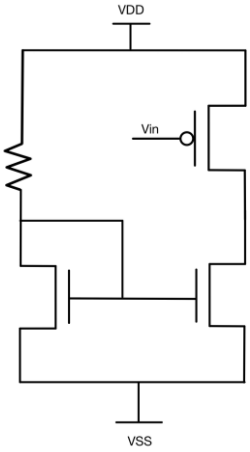

Figure 8: RGC Topology used in design

We incorporated two large resistors (as shown in Figure 9) to ensure that the transistors operate in the saturation region. This modification allowed us to switch to using NMOS transistors as the active devices, which is advantageous due to their higher mobility compared to PMOS transistors, resulting in better performance.

For the second gain stage, we applied the same design methodology. We initially set the current source to 4 mA and calculated g_m to achieve a gain of 4. Based on this, we carefully adjusted the W/L ratio to meet the gain requirements. After configuring these parameters, we ran a pole-zero (pz) simulation to identify the positions of the poles. To improve the frequency response, we focused on moving the dominant pole to higher frequencies by fine-tuning the design—specifically by reducing the current and adjusting the W/L ratio further. This approach helped us optimize both the gain and bandwidth of the second stage.

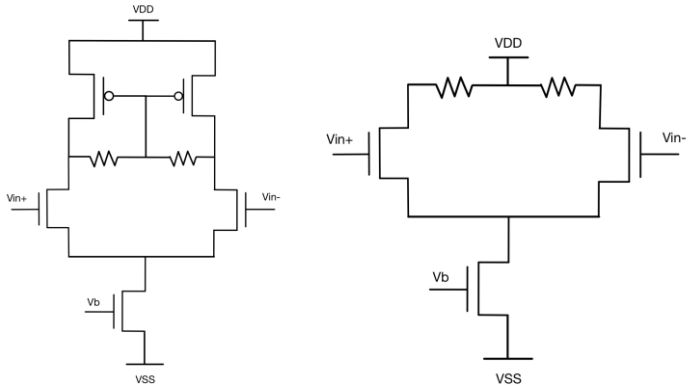

Figure 9: Large Gain Amplifiers

3. Simulations

3.1 Test Topology

As described in the design above, Figure 10 presents our final design topology, while Figure 11 illustrates the corresponding schematic with labeled parameters. The transistors and other technology-specific components used in the design were sourced from the cmrf8sf library. Common elements such as vdd, gnd, and voltage sources were selected from the analogLib library.

For the simulation, shows in Figure 12, we used a 2V power supply for V_{DD}. The photodiode model, as previously mentioned, is represented by an ideal current source in parallel with a 500fF shunt capacitance. We opted for a differential input to our TIA, which helps improve noise immunity and signal integrity. The differential output is designed to drive two 50Ω transmission lines, and to ensure DC isolation, we included two large capacitors in series with the transmission lines. This setup provides efficient signal transfer while maintaining proper isolation and stability.

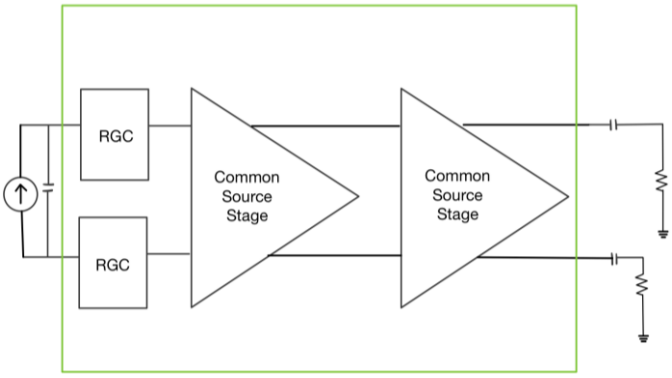

Figure 10: Final Design Topology

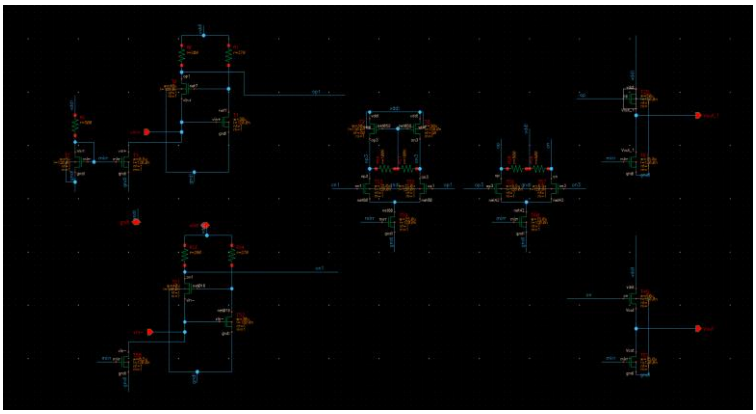

Figure 11: Design Circuit Schematic with labeled parameters

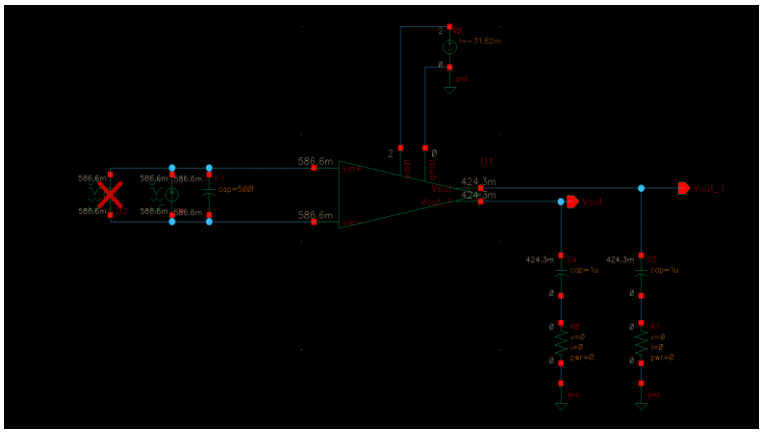

Figure 12: Test Schematic for differential output

3.2 Simulation Results

As shown in Figure 13, we measured the gain and bandwidth of our design, obtaining values of 2.55kΩ and 3.627GHz, respectively. These measurements demonstrate the efficiency of the design in terms of signal amplification and frequency response.

Figure 14 shows the output swing of the differential output, which ranges from -241.595 mV to 244.781 mV. This

range highlights the balanced nature of the differential signal and indicates a sufficient voltage swing for the designed circuit.

We recorded the signal between the capacitor and resistor of the output load. The measured slew rate of our design is approximately 8.892V/ns, which is sufficient for the intended performance. This result is illustrated in Figure 15, demonstrating the rapid response capability of the design.

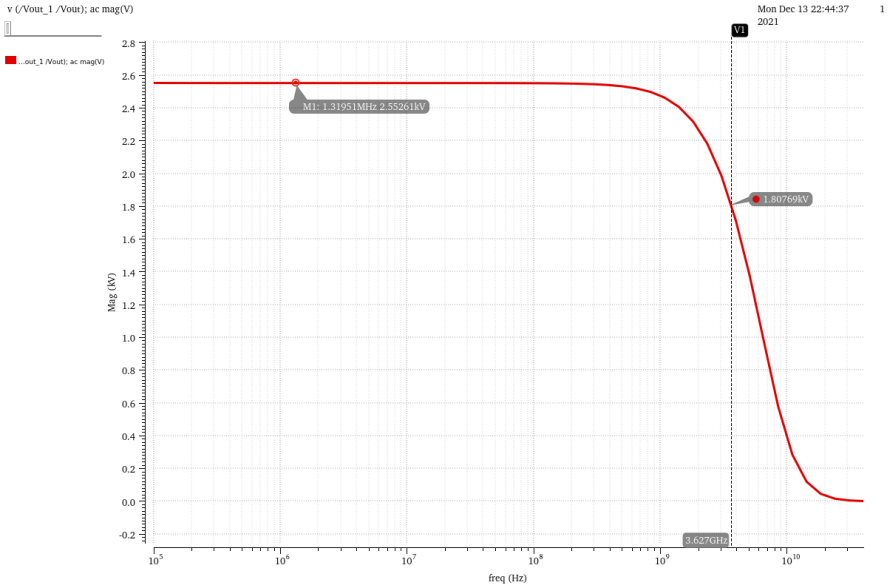

Figure 13: AC Transfer Characteristics Curve

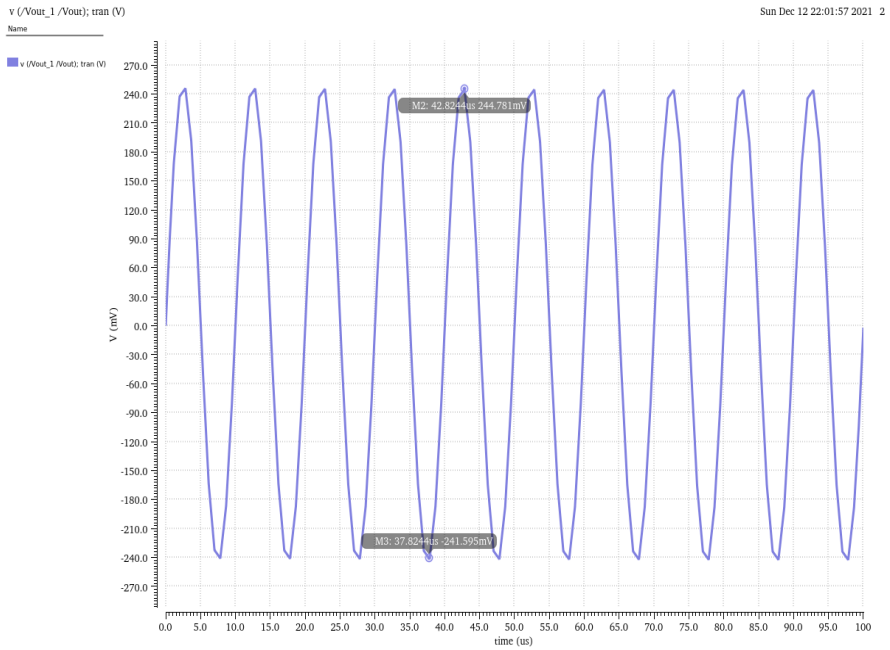

Figure 14: Transient Analysis Curve

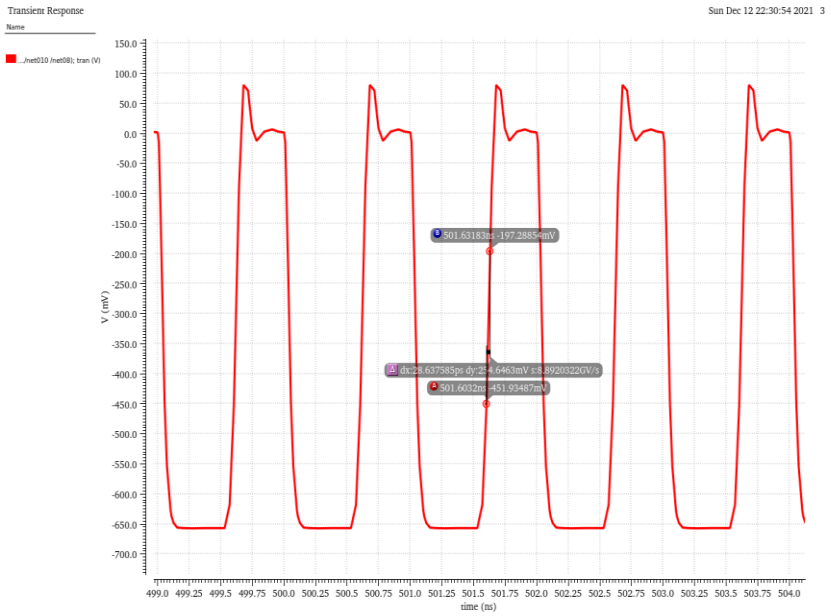

Figure 15: Slew Rate

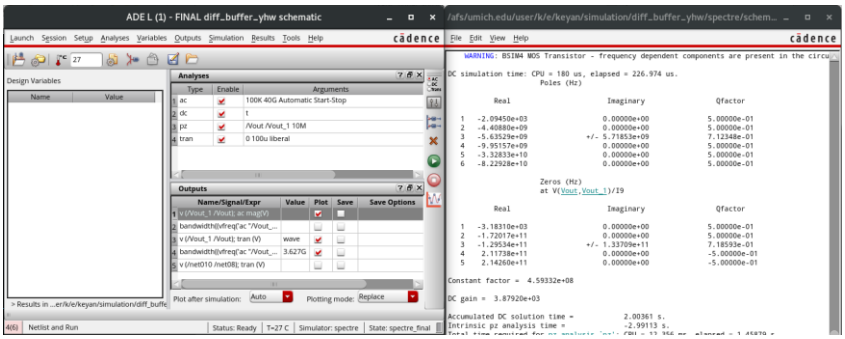

Figure 16: Calculated Poles and Zeros of Design

On the left side of Figure 16, we show the calculated bandwidth from the differential output, while the right side displays the poles and zeros. Notably, there are three significant poles ranging from 4.4GHz to 10GHz that greatly impact the bandwidth. To further improve this design, we could push these poles to higher frequencies, which would enhance the bandwidth and overall performance of the circuit.

At the DC operating points shown in Figure 17, the total DC current is measured at 31.82 mA. This results in a power consumption of approximately 63.64mW, which remains well below our target of 100mW.

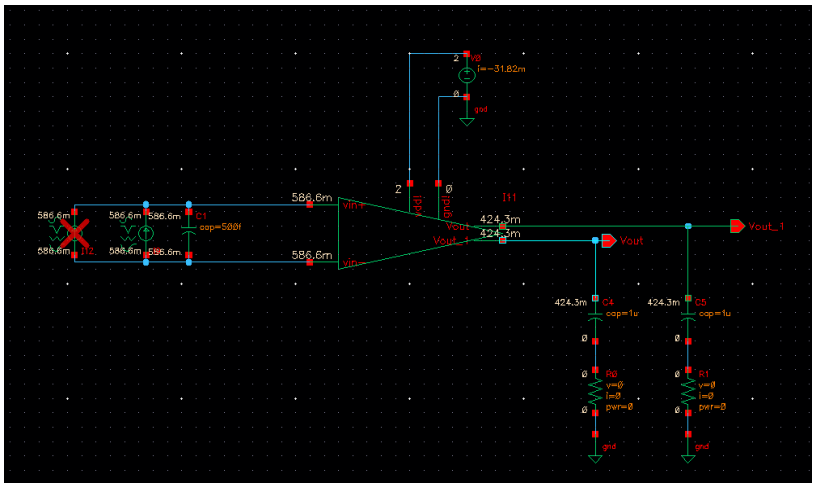

Figure 17: Power Consumption

3.3 Overall Performance

The method for calculating the estimated size of the design will be detailed in Part D. This section will cover the steps and considerations involved in determining the physical dimensions and layout, including factors such as transistor sizing, component placement, and overall chip area.

Objectives	Circuit Performance
Power Supply	2V
DC Power Dissipation	63.64mW
Transimpedance	2.55 kΩ
-3dB Bandwidth	3.627GHz
Differential output swing	±240 mV
Differential output slew rate	8.916V/ns
Output load on each differential output	50Ω
Input	Differential
Estimated Size	572.7746um^2

3.4 Detailed Size

We estimated the areas of our transistors and resistors by sketching their layouts and then summing them to calculate the total chip area. Based on these calculations, the estimated total area of the chip is 572.7746 μm^2. This approach provides a rough approximation of the physical space required for the design.

Component	Width (um)	Length (um)	Area (um^2)
R0, R23	1.75	1.1	1.925
R1, R24	1.69	1	1.69
R26, R27	0.2	49.5	9.18
R28, R29	1.4	2.1	2.94
R2	1.4	1.7	2.38
T9, T8 (pmos)	30	0.12	36.552
T2 (nmos)	5	0.12	6.522
T3, T58 (nmos)	8.5	0.12	10.93
T0, T51 (nmos)	40	0.12	49.36
T1, T52 (nmos)	30	0.12	37.16
T53, T55 (nmos)	12	0.12	15.20
T59 (nmos)	25	0.12	31.06
T56, T57 (nmos)	6.5	0.12	8.49
T60, T61, T62 (nmos)	15	0.12	18.86
T25, T46 (nmos)	50	0.12	61.56
VDD, VSS (19 in total)	1.22	0.27	0.3294

4. Conclusion

In conclusion, this paper details the successful design and implementation of a CMOS-based wide-bandwidth Transimpedance Amplifier (TIA) specifically for optical fiber communication at 5 Gbps. Our design of the differential Common-Source amplifier effectively meets the required specifications for gain, bandwidth, and power consumption. By carefully selecting components, adjusting parameters, and optimizing the layout, we achieved robust performance with a total chip area of 572.7746 μm^2. The calculated slew rate and output swing demonstrate the circuit's capability to efficiently handle the intended signals. Achieving a bandwidth of at least 3.5 GHz not only minimizes pattern-dependent jitter but also enhances the signal-to-noise ratio (SNR), which is crucial for maintaining signal integrity in high-speed optical links. Future improvements could focus on further enhancing the bandwidth by adjusting the pole positions. Overall, the results indicate a successful implementation of the design objectives, laying a solid foundation for further development and testing in next-generation optical communication systems.

5. Future Improvement

Increase Bandwidth: The current bandwidth of the circuit is somewhat limited, primarily because the gain of the Regulated Cascode (RGC) and buffer is approximately 250. This results in the need to achieve only a gain of 10 in the gain stage. As discussed in our analysis, we set the number of stages to 2, which only increased the bandwidth by 1.28 times its original value. Furthermore, the choice of a common-source amplifier as the gain stage contributes to an intrinsically lower bandwidth.

Implement Feedback: We could explore incorporating feedback mechanisms to enhance the bandwidth at the expense of some gain. This approach could potentially allow for better performance in high-speed applications while maintaining signal integrity.

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